REMARKS/ARGUMENTS

In the Office Action mailed April 14, 2009, claims 1 – 18 were rejected. In response, Applicant hereby requests reconsideration of the application in view of the amendments and the below-provided remarks. Claims 1 and 15 are amended. No claims are added or canceled.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-3, 9, and 14-18 were rejected under 35 U.S.C. 102(b) as being anticipated by Liu et al. (U.S. Pat. No. 6,219,797, hereinafter Liu). Additionally, claims 4-8 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Liu. Additionally, claims 10-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of the Applicant Admitted Prior Art (hereinafter AAPA). However, Applicant respectfully submits that these claims are patentable over Liu and the AAPA for the reasons provided below.

Independent Claim 1

Claim 1 is amended to particularly point out that a clock signal is generated at a next frequency in the sequence. As amended, claim 1 recites:

> "An electronic device for generating a clock signal for an integrated circuit, the device comprising:
> at least two clock generation elements configured to generate a single clock signal at a clock output in response to an input signal and to operate in a mutually exclusive manner, the outputs of said clock generation elements being selectively connectable to said clock output;
> means for receiving a data pattern representative of a sequence of frequencies at which said clock signal is required to be generated;
> means for causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at a next frequency in said sequence;
> means for causing the clock signal at the immediately previous frequency in said sequence to be disconnected from said clock output; and
> means for causing the clock signal at the next frequency in said sequence to be connected to said clock output;
> wherein the clock generation element being caused to generate a clock signal at each frequency in said sequence is independent of the value of said frequency" (emphasis added).

In contrast, Liu does not disclose "means for receiving a data pattern representative of a sequence of frequencies at which said clock signal is required to be generated". Liu merely discloses control bits CD0 and CD1 that are either at logic 0 or logic 1 (Liu, col. 21, lines 45-64). Even if the control bits CD0 and CD1 were understood to teach a data pattern, Liu nevertheless fails to disclose a "data pattern representative of a sequence of frequencies" (emphasis added). The control bits CD0 and CD1 of Liu "are used to select the output of one of the divide by circuits (÷2, ÷4, ÷64, ÷1024)" (Liu, col. 20, lines 12-14) and thus CD0 and CD1 are representative of only one state at a time, and not representative of a sequence of frequencies.

Additionally, Liu does not disclose "means for causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at a next frequency in said sequence." In contrast, Liu merely discloses a register bit "XTRG" (Liu, col. 19, lines 31-32) and Liu further discloses that "if 'XTRG' is set to be logic 1, an external crystal 70 of FIG. 5 will be the source to the system. Otherwise, if "XTRG" is set to be logic 0, internal ring oscillator 72 will be the source to the system" (Liu, col. 19, lines 33-36). However, Liu does not disclose that the source to the system is at "a next frequency in said sequence."

For the reasons presented above, Liu does not disclose all of the limitations of the claim because Liu does not disclose "means for receiving a data pattern representative of a sequence of frequencies at which said clock signal is required to be generated" and also does not disclose means for causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at a next frequency in said sequence." Accordingly, Applicant respectfully asserts claim 1 is not anticipated by Liu because Liu does not disclose all of the limitations of the claim.

Independent Claim 15

Applicant respectfully asserts independent claim 15 is not anticipated by Liu at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 15 recites "receiving a data pattern representative of a

sequence of frequencies at which said clock signal is required to be generated" (emphasis added). Additionally, claim 15 recites "causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at said next frequency" (emphasis added).

Here, although the language of claim 15 differs from the language of claim 1 and the scope of claim 15 should be interpreted independently of claim 1, Applicant respectfully asserts that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 15. Accordingly, Applicant respectfully asserts claim 15 is not anticipated by Liu because Liu does not disclose "receiving a data pattern representative of a sequence of frequencies at which said clock signal is required to be generated" and also does not disclose "causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at said next frequency," as recited in claim 15.

Dependent Claims 2-14 and 16-18

Claims 2-14 and 16-18 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 15. Applicant respectfully asserts that claims 2-14 and 16-18 are allowable at least based on allowable base claims. Additionally, each of claims 2-14 and 16-18 may be allowable for further reasons, as described below.

In regard to claim 2, Applicant respectfully submits that claim 2 is not anticipated by Liu because Liu does not disclose or suggest all of the limitations of the claim. Claim 2 recites that the "clock signal at the immediately previous frequency in said sequence is caused to be disconnected from said clock output prior to connection of the clock signal at the next frequency in the sequence to said clock output" (emphasis added). In contrast, Liu merely discloses that a "user can choose whether to use an external crystal oscillator or an on-chip internal ring oscillator" (Liu, col. 1, lines 40-42). However, Liu does not disclose or even suggest an "immediately previous frequency in said sequence" and a "next frequency in the sequence[.]" Accordingly, Applicant respectfully asserts that claim 2 is not anticipated by Liu because Liu does not disclose that a "clock signal at the

immediately previous frequency in said sequence is caused to be disconnected from said clock output prior to connection of the clock signal at the next frequency in the sequence to said clock output," as recited in claim 2.

In regard to claim 3, Applicant respectfully submits that claim 3 is also not anticipated by Liu at least for similar reasons to those stated above in regard to the rejection of claim 2. In particular, claim 3 recites that "generation of the clock signal at said next frequency in said sequence is commenced prior to disconnection of the clock signal at the immediately previous frequency in the sequence from the clock output" (emphasis added). Here, although the language of claim 3 differs from the language of claim 2 and the scope of claim 3 should be interpreted independently of claim 2, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 2 also apply to the rejection of claim 3. Accordingly, Applicants respectfully assert claim 3 is not anticipated by Liu because Liu does not disclose that "generation of the clock signal at said next frequency in said sequence is commenced prior to disconnection of the clock signal at the immediately previous frequency in the sequence from the clock output," as recited in claim 3.

In regard to claims 4 and 5, Applicant respectfully submits that claims 4 and 5 are patentable over Liu at least for similar reasons to those stated above in regard to the rejection of claim 2. In particular, claims 4 and 5 recite the "sequence". Here, although the language of claims 4 and 5 differs from the language of claim 2 and the scope of claims 4 and 5 should be interpreted independently of claim 2, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 2 also apply to the rejection of claims 4 and 5. Accordingly, Applicants respectfully assert claims 4 and 5 are patentable over Liu because Liu does not teach or suggest the "sequence," as recited in claims 4 and 5.

In regard to claims 7 and 8, Applicant respectfully submits that claims 7 and 8 are also patentable over Liu because Liu does not teach or suggest all of the limitations of the claims. Claim 7 recites a "variable programmable delay element for receiving data representative of the duration of a clock cycle of each frequency in said sequence" (emphasis added). Claim 8 depends from claim 7 and, hence, includes the same limitation through dependency. In contrast, Liu merely discloses a register bit "XTRG",

which allows the user to choose whether the external crystal or the internal ring oscillator will be the source to the system (Liu, col. 19, lines 31-36). Liu also discloses that the "control bits, CD1 and CD0 are used to select the output of one of the divide by circuits (÷2, ÷4, ÷64, ÷1024)" (Liu, col. 21, lines 45-64). However, Liu does not teach or suggest data representative of the duration of a clock cycle of each frequency in the sequence. Accordingly, Applicant respectfully asserts that claims 7 and 8 are patentable over Liu because Liu does not teach or suggest a "variable programmable delay element for receiving data representative of the duration of a clock cycle of each frequency in said sequence," as recited in claim 7.

In regard to claims 9 and 14, the Office Action fails to explain why the claimed limitations of claims 9 and 14 would have been anticipated by Liu because the Office Action does not acknowledge the actual language of claims 9 and 14. In particular, the Office Action fails to acknowledge that claim 9 recites that the "data pattern is derived from, or comprises, a series of requests for a change of frequency of said clock signal" (emphasis added). Additionally, the Office Action fails to acknowledge that claim 14 recites that the device is "arranged and configured to temporarily disconnect all of the clock generation elements from the clock output, in response to a request to do so" (emphasis added). In fact, the Office Action does not even make an assertion that the cited references might disclose the indicated limitation. Accordingly, Applicant respectfully asserts that claim 9 is not anticipated by Liu because Liu does not disclose that the "data pattern is derived from, or comprises, a series of requests for a change of frequency of said clock signal," as recited in claim 9. Additionally, Applicant respectfully asserts that claim 14 is not anticipated by Liu because Liu does not disclose a device "arranged and configured to temporarily disconnect all of the clock generation elements from the clock output, in response to a request to do so," as recited in claim 14.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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